

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

## TC74HC259AP, TC74HC259AF, TC74HC259AFN

### 8-Bit Addressable Latch

The TC74HC259A is a high speed CMOS ADDRESSABLE LATCH fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The respective bits are controlled by address inputs A, B, and C. When  $\overline{\text{CLEAR}}$  input is held high and enable input  $\overline{\text{G}}$  is held low, the data is written into the bit selected by address inputs, the other bits hold their previous conditions.

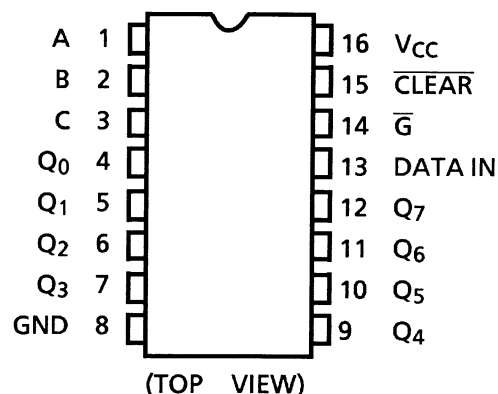
When both  $\overline{\text{CLEAR}}$  and  $\overline{\text{G}}$  held high, writing of all bits is inhibited regardless of address inputs, and their previous condition are held. When  $\overline{\text{CLEAR}}$  is held low and  $\overline{\text{G}}$  is held high, all bits are reset to low regardless of the other inputs. When both of  $\overline{\text{CLEAR}}$  and  $\overline{\text{G}}$  held low, all bits which isn't selected by address inputs are reset to low.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

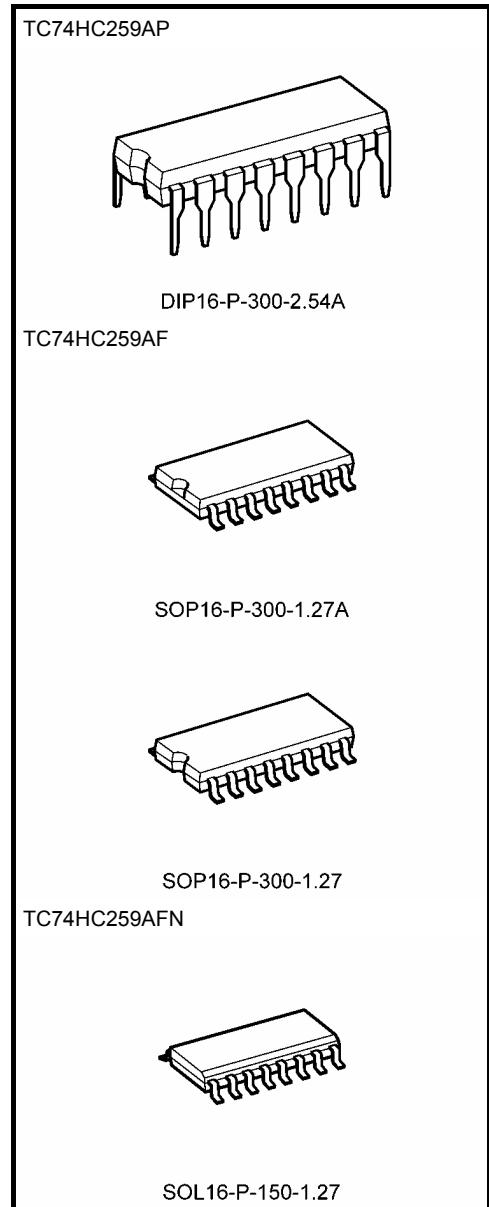
### Features

- High speed:  $t_{pd} = 15 \text{ ns}$  (typ.) at  $V_{CC} = 5 \text{ V}$
- Low power dissipation:  $I_{CC} = 4 \mu\text{A}$  (max) at  $T_a = 25^\circ\text{C}$
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (min)
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance:  $|I_{OH}| = I_{OL} = 4 \text{ mA}$  (min)
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range:  $V_{CC} (\text{opr}) = 2\sim 6 \text{ V}$
- Pin and function compatible with 74LS259

### Pin Assignment

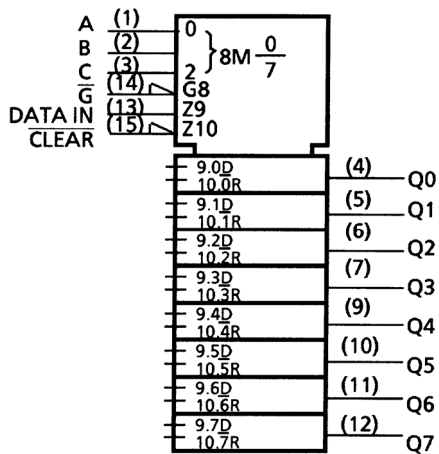


Note: xxxFN (JEDEC SOP) is not available in Japan.



Weight	
DIP16-P-300-2.54A	: 1.00 g (typ.)
SOP16-P-300-1.27A	: 0.18 g (typ.)
SOP16-P-300-1.27	: 0.18 g (typ.)
SOL16-P-150-1.27	: 0.13 g (typ.)

## IEC Logic Symbol



## Truth Table

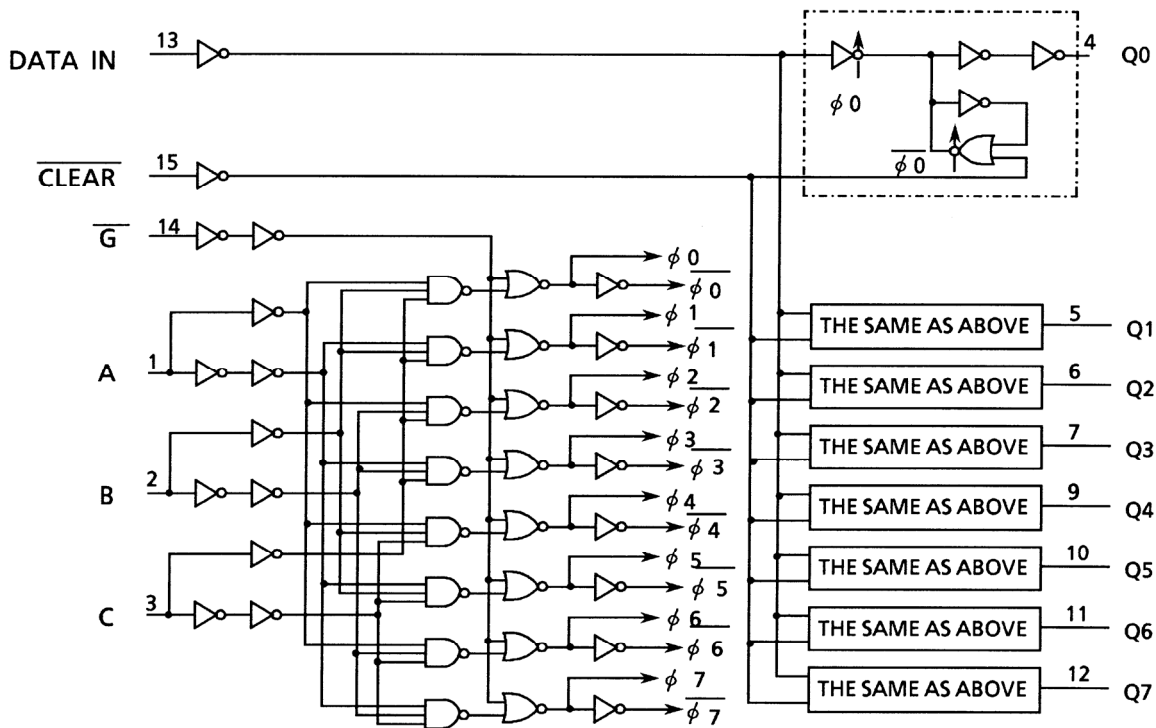
Inputs		Output of Addressed Latch	Each Other Output	Function
CLEAR	$\bar{G}$			
H	L	D	QiO	Addressable Latch
H	H	QiO	QiO	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear All Bits to "L"

Select Inputs			Latch Addressed
C	B	A	
L	L	L	Q0
L	L	H	Q1
L	H	L	Q2
L	H	H	Q3
H	L	L	Q4
H	L	H	Q5
H	H	L	Q6
H	H	H	Q7

D: The level at the data input.

QiO: The level before the indicated steady-state input conditions were established ( $i = 0, 1, \dots, 7$ )

## System Diagram



## Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5~7.0	V
DC input voltage	$V_{IN}$	-0.5~ $V_{CC} + 0.5$	V
DC output voltage	$V_{OUT}$	-0.5~ $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	$\pm 20$	mA
Output diode current	$I_{OK}$	$\pm 20$	mA
DC output current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 50$	mA
Power dissipation	$P_D$	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	$T_{stg}$	-65~150	$^{\circ}C$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Note 2: 500 mW in the range of  $T_a = -40\sim 65^{\circ}C$ . From  $T_a = 65$  to  $85^{\circ}C$  a derating factor of  $-10$  mW/ $^{\circ}C$  should be applied until 300 mW.

## Recommended Operating Conditions (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2~6	V
Input voltage	$V_{IN}$	0~ $V_{CC}$	V
Output voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating temperature	$T_{opr}$	-40~85	°C
Input rise and fall time	$t_r, t_f$	0~1000 ( $V_{CC} = 2.0$ V) 0~500 ( $V_{CC} = 4.5$ V) 0~400 ( $V_{CC} = 6.0$ V)	ns

Note: The recommended operating conditions are required to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

## Electrical Characteristics

### DC Characteristics

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			$T_a = -40\sim 85^\circ\text{C}$		Unit	
				Min	Typ.	Max	Min	Max		
High-level input voltage	$V_{IH}$	—	2.0	1.50	—	—	1.50	—	V	
			4.5	3.15	—	—	3.15	—		
			6.0	4.20	—	—	4.20	—		
Low-level input voltage	$V_{IL}$	—	2.0	—	—	0.50	—	0.50	V	
			4.5	—	—	1.35	—	1.35		
			6.0	—	—	1.80	—	1.80		
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20 \mu\text{A}$	2.0	1.9	2.0	—	1.9	—	V
			$I_{OH} = -4 \text{ mA}$	4.5	4.4	4.5	—	4.4	—	
			$I_{OH} = -5.2 \text{ mA}$	6.0	5.9	6.0	—	5.9	—	
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20 \mu\text{A}$	2.0	—	0.0	0.1	—	0.1	V
			$I_{OL} = 4 \text{ mA}$	4.5	—	0.0	0.1	—	0.1	
			$I_{OL} = 5.2 \text{ mA}$	6.0	—	0.0	0.1	—	0.1	
Input leakage current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	6.0	—	—	$\pm 0.1$	—	$\pm 1.0$	$\mu\text{A}$	
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	6.0	—	—	4.0	—	40.0	$\mu\text{A}$	

### Timing Requirements (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40 ~85°C	Unit	
			V <sub>CC</sub> (V)	Typ.	Limit		
Minimum pulse width ( $\overline{G}$ )	$t_W$ (L)	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum pulse width ( $\overline{CLEAR}$ )	$t_W$ (L)	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time (DATA)	$t_s$	—	2.0	—	50	60	ns
			4.5	—	10	12	
			6.0	—	9	11	
Minimum set-up time (A, B, C)	$t_s$	—	2.0	—	25	30	ns
			4.5	—	5	6	
			6.0	—	5	5	
Minimum hold time (DATA)	$t_h$	—	2.0	—	25	30	ns
			4.5	—	5	6	
			6.0	—	5	5	
Minimum hold time (A, B, C)	$t_h$	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	

### AC Characteristics ( $C_L = 15$ pF, $V_{CC} = 5$ V, $T_a = 25^\circ\text{C}$ , input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	$t_{TLH}$	—	—	4	8	ns
	$t_{THL}$					
Propagation delay time (DATA-Q)	$t_{pLH}$	—	—	15	22	ns
	$t_{pHL}$					
Propagation delay time (A, B, C-Q)	$t_{pLH}$	—	—	21	32	ns
	$t_{pHL}$					
Propagation delay time ( $\overline{G}$ -Q)	$t_{pLH}$	—	—	16	28	ns
	$t_{pHL}$					
Propagation delay time ( $\overline{CLEAR}$ -Q)	$t_{pHL}$	—	—	13	23	ns

## AC Characteristics ( $C_L = 50 \text{ pF}$ , input: $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40~85°C		Unit
				Min	Typ.	Max	Min	Max	
Output transition time	$t_{TLH}$ $t_{THL}$	—	2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation delay time (DATA-Q)	$t_{pLH}$ $t_{pHL}$	—	2.0	—	56	130	—	165	ns
			4.5	—	18	26	—	33	
			6.0	—	15	22	—	28	
Propagation delay time (A, B, C-Q)	$t_{pLH}$ $t_{pHL}$	—	2.0	—	83	185	—	230	ns
			4.5	—	25	37	—	46	
			6.0	—	21	31	—	39	
Propagation delay time ( $\overline{G}$ -Q)	$t_{pLH}$ $t_{pHL}$	—	2.0	—	67	165	—	205	ns
			4.5	—	20	33	—	41	
			6.0	—	17	28	—	35	
Propagation delay time ( $\overline{\text{CLEAR}}$ -Q)	$t_{pHL}$	—	2.0	—	52	135	—	170	ns
			4.5	—	16	27	—	34	
			6.0	—	14	23	—	29	
Input capacitance	C <sub>IN</sub>	—	—	5	10	—	10	pF	
Power dissipation capacitance	C <sub>PD</sub> (Note)	—	—	35	—	—	—	pF	

Note: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

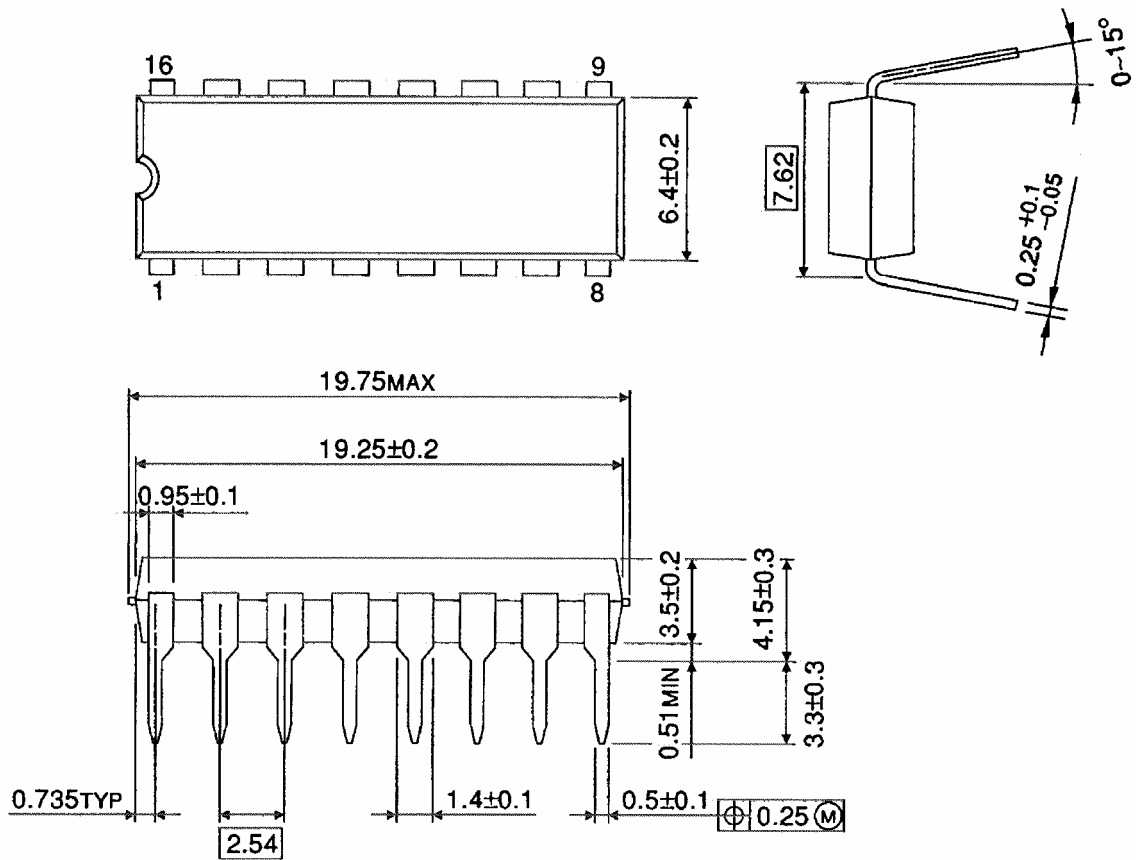
Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

## Package Dimensions

DIP16-P-300-2.54A

Unit : mm

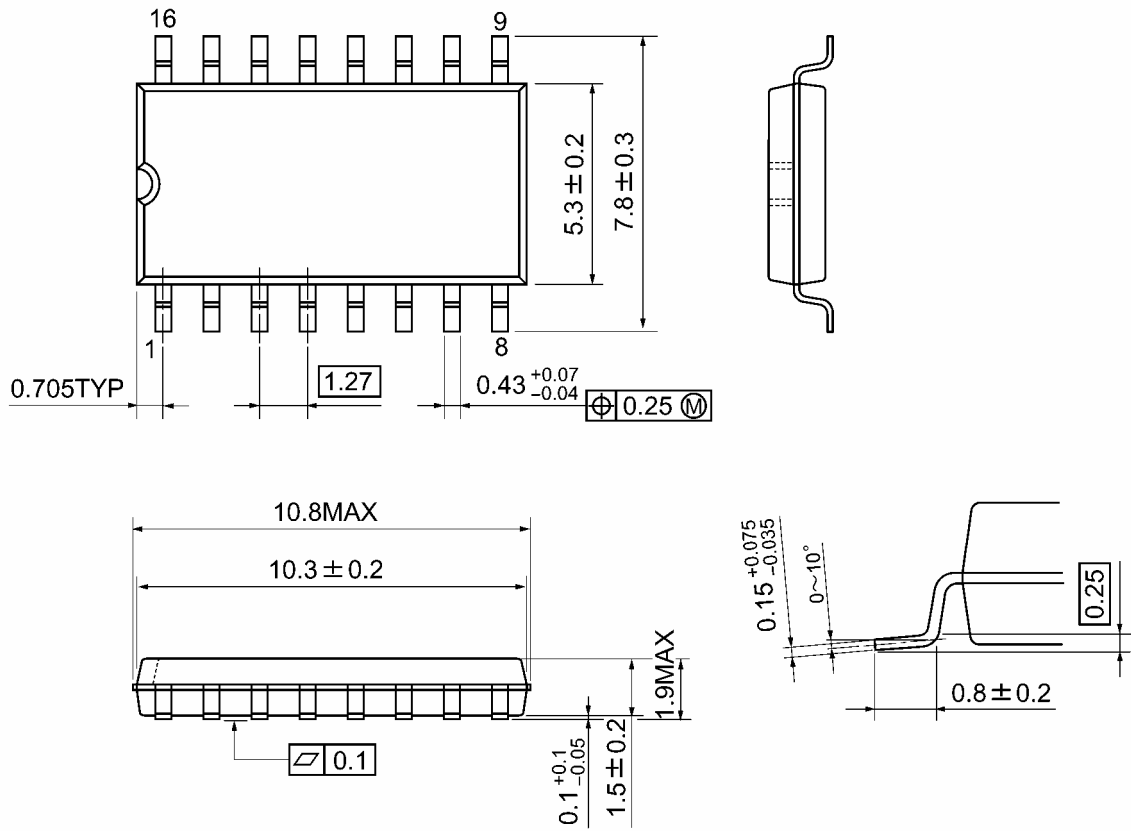


Weight: 1.00 g (typ.)

**Package Dimensions**

SOP16-P-300-1.27A

Unit: mm



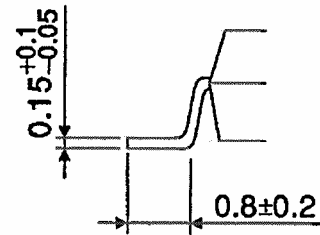
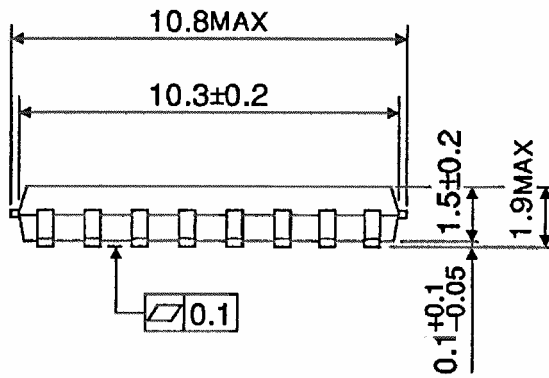
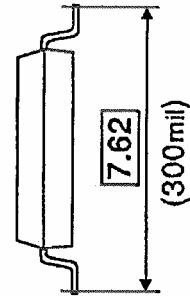
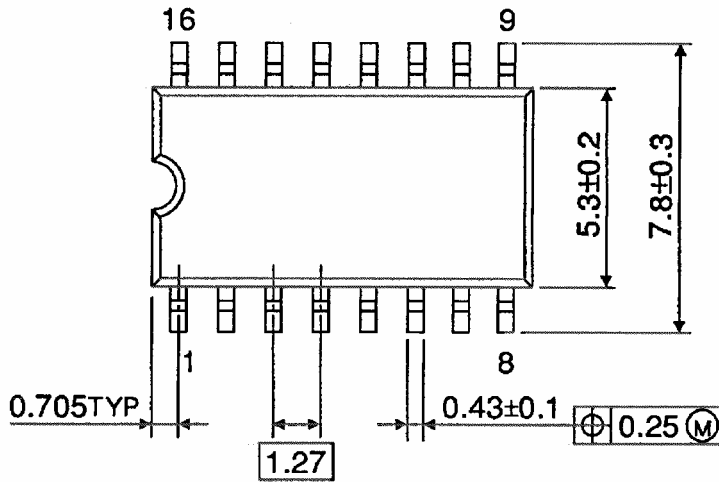
Weight: 0.18 g (typ.)



## Package Dimensions

SOP16-P-300-1.27

Unit : mm

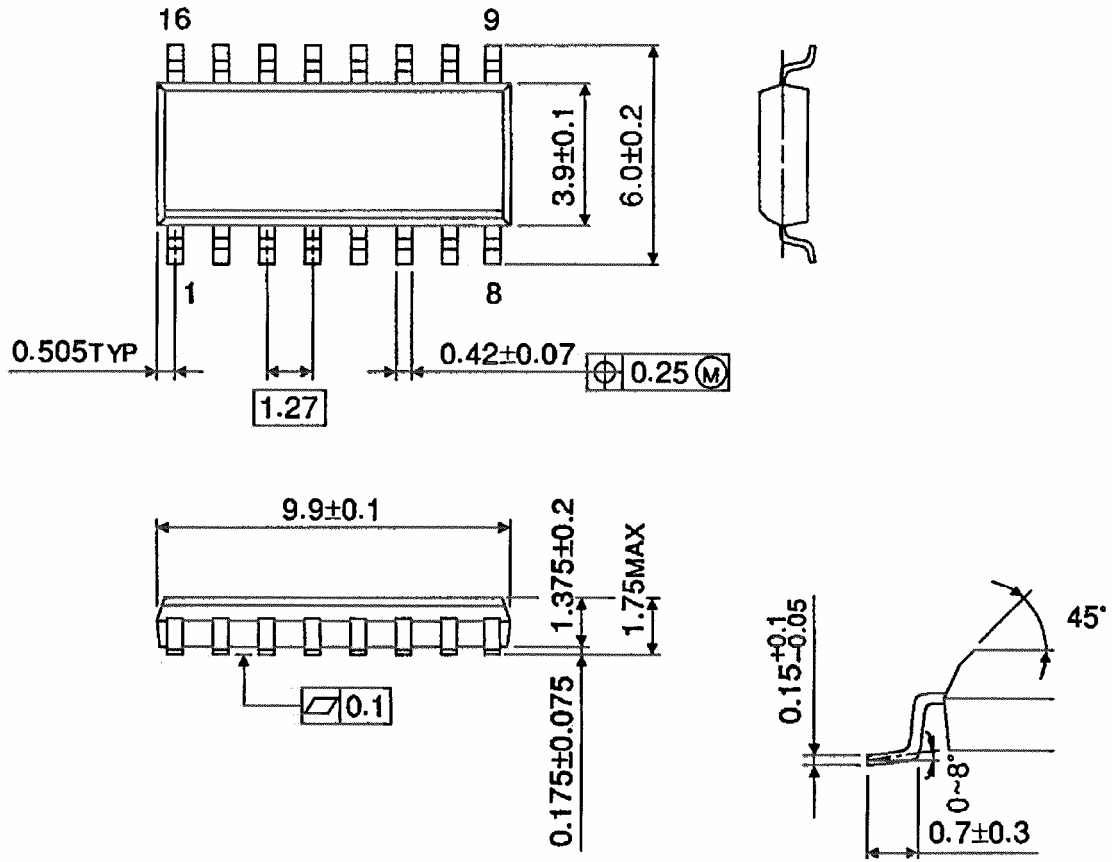


Weight: 0.18 g (typ.)

Package Dimensions (Note)

SOL16-P-150-1.27

Unit : mm



Note: This package is not available in Japan.

Weight: 0.13 g (typ.)

**Note: Lead (Pb)-Free Packages****DIP16-P-300-2.54A SOP16-P-300-1.27A SOL16-P-150-1.27****RESTRICTIONS ON PRODUCT USE**

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